CLAIMS

What is claimed is:

1. A memory to provide off boundary memory access, comprising:

a right memory array having a plurality of right memory rows;

a left memory array having a plurality of left memory rows;

a plurality of row lines each having a right memory row and left memory row, respectively; and

an off boundary row address decoder coupled to the right and left memory arrays, the off boundary row address decoder to perform an off boundary memory access.

2. The memory of claim 1, wherein,

the memory is an off boundary memory.

3. The memory of claim 1, wherein,

the off boundary memory access includes

accessing a desired plurality of memory addresses from one of a right or left memory row of a row line and from one of a left or right memory row of an adjacent row line.

4. The memory of claim 1, wherein,

the off boundary memory access to be performed within one memory access cycle.

5. The memory of claim 1, wherein,

the off boundary row address decoder to select appropriate right and left memory rows based upon a starting address and a sequence number to access the desired plurality of memory addresses.

6. The memory of claim 1, further comprising:

a column select decoder to select appropriate bit columns of right and left memory rows based upon a starting address and a sequence number to access the desired plurality of memory addresses.

7. The memory of claim 1, wherein,

the off boundary row address decoder further includes a plurality of row decoders, each row decoder coupled to a respective left and right memory row of a row line, the row decoder to decode an address to access the desired plurality of memory addresses data within the respective left and right memory row of the row line.

8. The memory of claim 7, wherein,

each row decoder is coupled to at least one adjacent row decoder.

9. The memory of claim 8, wherein,

each row decoder is coupled to the at least one adjacent row decoder by a multiplexer.

10. The memory of claim 9, wherein,

the off boundary row address decoder further includes

an off boundary detector coupled to each of the multiplexers.

11. The memory of claim 10, wherein

based upon a starting address and a sequence number, the off boundary detector to determine whether an off boundary memory access is needed, and if so, the off boundary memory detector to generate an off boundary signal to control the multiplexers.

12. The memory of claim 11, wherein,

the off boundary signal to control the multiplexers in that after the memory addresses from one of a right or left memory row of a first row line selected by a row decoder are accessed,

then the appropriate memory addresses from one of a left or right memory row of an adjacent row line to be accessed by an adjacent row decoder.

13. A signal processor comprising:

at least one signal processing unit, the at least one signal processing unit coupled to an off boundary memory by a data bus,

the off boundary memory including

a right memory array having a plurality of right memory rows;

a left memory array having a plurality of left memory rows;

a plurality of row lines each having a right memory

row and left memory row, respectively; and

an off boundary row address decoder coupled to the right and left memory arrays, the off boundary row address decoder to perform an off boundary memory access.

14. The signal processor of claim 13, wherein,

the signal processor is a digital signal processor to perform digital signal processing instructions.

15. The signal processor of claim 13, wherein,

the off boundary memory access includes

accessing a desired plurality of memory addresses from one of a right or left memory row of a row line and from one of a left or right memory row of an adjacent row line.

16. The signal processor of claim 13, wherein,

the off boundary memory access to be performed within one memory access cycle.

17. The signal processor of claim 13, wherein,

the off boundary row address decoder to select appropriate right and left memory rows based upon a starting address and a sequence number to access the desired plurality of memory addresses.

18. The signal processor of claim 13, further comprising:

a column select decoder to select appropriate bit columns of right and left memory rows based upon a starting address and a sequence number to access the desired plurality of memory

addresses.

19. The signal processor of claim 13, wherein, the off boundary row address decoder further includes

a plurality of row decoders, each row decoder coupled to a respective left and right memory row of a row line, the row decoder to decode an address for accessing the desired plurality of memory addresses data within the respective left and right memory row of the row line.

20. The signal processor of claim 19, wherein,

each row decoder is coupled to at least one adjacent row decoder.

21. The signal processor of claim 20, wherein,

each row decoder is coupled to the at least one adjacent row decoder by a multiplexer.

22. The signal processor of claim 21, wherein,

the off boundary row address decoder further includes

an off boundary detector coupled to each of the multiplexers.

23. The signal processor of claim 22, wherein

based upon a starting address and a sequence number, the off boundary detector to determine whether an off boundary memory access is needed, and if so,

the off boundary detector to generate an off boundary signal to control the multiplexers.

24. The signal processor of claim 23, wherein,

the off boundary signal to control the multiplexers in that after the memory addresses from one of a right or left memory row of a first row line selected by a row decoder are accessed,

then the appropriate memory addresses from one of a left or right memory row of an adjacent row line are accessed by an adjacent row decoder.

25. A method to provide off boundary memory access in a memory, the method comprising:

apportioning a memory into a right memory array having a plurality of right memory rows and a left memory array having a plurality of left memory rows;

defining a plurality of row lines each having a right memory row and left memory row, respectively; and

performing an off boundary memory access by accessing a desired plurality of memory addresses from one of a right or left memory row of a row line and from one of a left or right memory row of an adjacent row line.

26. The method of claim 25, wherein,

the off boundary memory access is performed within one memory access cycle.

27. The method of claim 25, further comprising:

selecting appropriate right and left memory rows based upon a starting address and a sequence number to access the desired plurality of memory addresses.

28. The method of claim 25, further comprising:

selecting appropriate bit columns of right and left memory rows based upon a starting address and a sequence number to access the desired plurality of memory addresses.

29. The method of claim 25, further comprising:

decoding an address for accessing the desired plurality of memory addresses data within a respective left and right memory row of a row line.

30. The method of claim 29, further comprising:

coupling each row line to at least one adjacent row line by a multiplexer.

31. The method of claim 30, further comprising:

determining whether an off boundary memory access is needed based upon a starting address and a sequence number, and if so,

generating an off boundary signal to control the multiplexers.

32. The method of claim 31, wherein,

the off boundary signal controls the multiplexers in that after the memory addresses from one of a right or left memory row of a first row line are accessed,

then the appropriate memory addresses from one of a left or right memory row of an adjacent row line are accessed.